What is claimed is:

1. A method for synchronizing all clock sources of semiconductor devices, comprising:

(a) generating multiple clock sources in a plurality of semiconductor devices;

(b) designating one semiconductor device having a clock source with the lowest rate clock signal as a master device and other devices as slave devices when the multiple clock sources are stable;

(c) designating the lowest rate clock signal of the master device as a reference clock source;

(d) performing, according to the reference clock source, a phase-aligned check on other clock sources in the master device, such that other clock sources of the master device are synchronized with the reference clock source to generate a zeroing signal;

(e) respectively performing, according to the zeroing signal, a phase-aligned check on a local lowest rate clock source in each slave device, such that all local lowest rate clock sources of the slave devices are synchronized with the lowest rate clock signal of the master device to respectively generate an aligning signal; and

(f) respectively performing, according to the aligning signal, a phase-aligned check on other clock sources in each slave device, such that other clock sources of each slave device are separately synchronized with the local lowest rate clock

signal of the respective slave devices, thereby completing clock synchronization for the plurality of semiconductor devices.

2. The method according to claim 1, wherein the plurality of semiconductor devices are implemented by Field Programmable Gate Array (FPGA) or Application Specific Integrated Circuit (ASIC).

3. The method according to claim 1, wherein the clock generators are implemented by delay locked loop (DLL) or digital clock manager (DCM).

4. The method according to claim 1, wherein step (d) further comprises: (d1) triggering a phase checker in the master device to sample the clock sources inside the master device for phase alignment comparison by means of rising or falling edges of an external input clock source; (d2) outputting the zeroing signal to concurrently signal each slave device when all phases are aligned; and (d3) otherwise, outputting a reset signal reset to re-generate multiple clock sources for re-alignment operation.

5. The method according to claim 1, wherein step (e) further comprises: (e1) respectively checking the lowest rate clock source of the master device through an external phase checker in each slave device to determine if the zeroing signal has been sent; (e2) respectively performing a phase-aligned check on each slave device through a respective external phase checker when the zeroing signal is received and all clock sources in each slave device are

stable; (e3) respectively sending the aligning signal to indicate a phase alignment and clock synchronization for the lowest rate clock signal of the master device and the local lowest rate clock signal of the respective slave device when all phases are aligned; and (e4) otherwise, sending a reset signal to re-generate the local lowest rate clock signal of the respective slave device and then repeat step (e1).

6. The method according to claim 1, wherein step (f) further comprises: (f1) respective internal phase checkers in each slave device determining if a respective external phase checker has sent the aligning signal; (f2) respective internal phase checkers performing the phase-aligned check in a respective slave device when the aligning signal is received and all clock sources in the respective slave device are stable; (f3) sending the aligning signal to indicate a phase alignment for the clock sources in the respective slave device and a clock synchronization for the semiconductor devices when all phases are aligned; and (f4) otherwise, sending a reset signal reset to respectively re-generate the multiple clock sources, except the local lowest rate clock source, of the respective slave device and then repeat step (f1).

7. A system for synchronizing all clock sources of semiconductor devices, comprising:

a first semiconductor device having a phase checker and a multi-clock generator including generation of the lowest rate clock source, wherein the phase checker performs phase alignment according to the lowest rate clock source, such that multiple

clock sources generated by the multi-clock generator are synchronized and thus a zeroing signal is output;

a plurality of second semiconductor devices, each having an external phase checker, an internal phase checker and a multi-clock generator including generation of a clock-aligned source, wherein the external phase checker performs phase alignment according to the zeroing signal, such that the lowest rate clock source and the clock-aligned source have phase synchronization to thus output an aligning signal to the internal phase checker for phase alignment, thereby synchronizing multiple clock sources generated by each second semiconductor, and thus completing clock synchronization of all semiconductor devices.

8. The system according to claim 7, wherein the semiconductor devices are Field Programmable Gate Arrays (FPGAs) or Application Specific Integrated Circuits (ASICs).

9. The system according to claim 7, wherein the clock generators are delay locked loop (DLLs) or digital clock managers (DCMs).